A 46µW Self-Calibrated GHz VCO for Low Power Radios

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Abstract—This brief presents a 46µW 0.8-2GHz tunable oscillator with built-in self-calibrated PVT compensation for applications in low power radios. With single-point current calibration at room temperature, the proposed VCO achieves 2.24% frequency accuracy against process variation, 1.6% frequency shift over 0.85-1.15V supply voltage, and 167ppm/°C temperature sensitivity between -7°C and 76°C. The sub-135pJ on-chip self-calibration is based on a successive approximation scheme. Our design shows 3.4x improved process variation tolerance, 45x improved supply sensitivity, and 5.2x improved temperature sensitivity, as compared to the free-running VCO without self-calibration. Measurements are taken from 94 chips fabricated in two different lots in TSMC 65nm CMOS process.

Index Terms—CMOS, low power, ring oscillator, voltage controlled oscillators, PVT compensation.

I. INTRODUCTION

Low power radio systems, such as UWB impulse radios and wake-up receivers, have attracted attention for applications in wireless sensor networks (WSN) and body area networks (BAN), where low power operation at low cost is required. Generating an accurate local frequency reference is critical in these systems, as it often sets the limit of achievable power savings [1] and receiver sensitivity [2], determines the optimal frequency plan [3], and affects network dynamics [4]. Hence, an oscillator immune to variations of process, supply voltage, and temperature (PVT) is extremely desirable. In addition to the accuracy requirement, the oscillator must operate under a stringent power budget (<100µW) and be inexpensive to integrate within a state-of-the-art CMOS process.

The ring oscillator based voltage-controlled oscillator (VCO) exhibits wide-tuning range, low power consumption, small die area, and ease of integration. Compared to the more power hungry LC oscillator [5] and the FBAR-based resonator with limited tuning range [6], it is particularly suitable for low power radios whose inherent architecture is more tolerant to phase noise but require flexible low power operation. Unfortunately, the ring oscillator suffers from severe impacts of increasing variability, especially as CMOS technology scales down to the nanometer regime. Despite efforts to improve the inherent accuracy of free-running oscillators through symmetric loads [7], stable current bias [8], and threshold and temperature sensing [9], built-in self-calibration circuitry and compensation schemes are needed to achieve enhanced performance against PVT variations as demanded in practical low power radios.

In this brief, we demonstrate a 46µW VCO with built-in self-calibrated PVT compensation that can function both as a local oscillator (LO) [3] and as a wake-up clock [1]. The proposed oscillator has a tuning range of 0.8-2GHz that allows flexible channel selection and frequency hopping. Based on the successive approximation method [10], the self-calibration incorporated in our VCO design improves the frequency sensitivity of the free-running oscillator to process by 3.4x, to supply voltage by 45x, and to temperature by 5.2x, while consuming less than 135pJ to perform the calibration procedure. These results are verified by more than 94 test chips from two different lots fabricated in TSMC 65nm CMOS process.

II. PVT COMPENSATION FOR VCO

Three types of built-in calibration techniques have been proposed for PVT compensation in VCO’s: closed-loop control voltage monitoring [11], digital counter over fixed time [12], [13], and analog time-to-voltage conversion (TVC) [14].

Monitoring the control voltage in closed-loop configuration requires long settling time and continuous loop operation. At the same time, counting over a fixed time window takes more calibration time to arrive at the same frequency resolution than the analog TVC technique. Hence the most energy-efficient calibration is realized with analog TVC that is able to track the frequency within several cycles of oscillation.

For low power radio applications in WSN and implantable electronics, integration cost, power consumption, and form factor make an external reference, such as a crystal oscillator, undesirable. Without such frequency references, we employ absolute comparison with low-tolerance on-chip components for calibration, instead of relative frequency comparison [14].

Given the design considerations mentioned above, we use the analog TVC technique based on absolute comparison in our self-calibration circuitry with post-fabrication trimming. To further minimize test time and cost, single-point DC current

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and VTVC are then compared to update the digital code (D ctrl) stored in the SAR to generate V ctrl. With each comparison and (RST), until Conv_Request triggers the self-calibration. As the divider ratio). The system starts in the Sleep/RST state with variable resistive divider from V DD in our measurement, when the calibration is completed, the final Dctrl is stored in the SAR to generate the optimal Vctrl.

If the accuracy of V TVC against PVT variation, an optimal block implementation in the self-calibration system so that the contributions from other variation terms are minimized.

The TVC measures the oscillation period, and its absolute accuracy is especially critical. It is realized with a current source (I ref) charging up a pF capacitor, as illustrated in Fig. 3(a). CLK is generated by a divider after the VCO, and it has a 50-50 duty cycle and a period of 2NT osc. The output voltage V TVC at the end of each charging period equals LV ref T osc/C. To ensure the accuracy of V TVC against PVT variation, an addition-based current source with temperature compensation and linear supply dependence [8] is employed. This current source is fully-integrated and does not require a bandgap reference as shown in Fig. 3(b). I ref in Fig. 3(b) is calibrated each bit in D ctrl resolves from MSB to LSB, f VCO approaches its final value at increasingly finer steps. The decision of LSB in D ctrl indicates the completion of the calibration and returns the system back to RST state with f VCO locked to its calibrated value.

We zoom into the dashed box to show the state transitions and the progression of D ctrl, V TVC, and the comparator output V CP, as the first 2 bits resolve. Following Conv_Request, the system first enters the Preload state (P) to load the initial code “100…0” in the SAR before starting the bit cycle at MSB. Each bit cycle consists of 3 phases—Update (U), Sample (S), and Compare (C) phases. During Sample, V TVC linearly increases with time, as I ref charges up the capacitor inside the TVC. V TVC is then held stable and compared with V IN in the Compare phase, and the comparator decision V CP updates the active bit of the SAR in the Update phase of the next bit cycle. Update is also used to discharge V TVC for the next Sample phase.

In addition to power-up, the self-calibration is performed periodically with a self-timer. Need-based calibration can also be realized using a low-power temperature sensor to trigger Conv_Request, though it is not implemented in our system.

### C. Frequency Accuracy

The input offset of the comparator (V CP,off), the finite resolution of the SAR and the DAC (V LSB), and the capacitor variation in the TVC determine the final calibrated frequency accuracy:

\[
\left( \frac{\sigma_f}{f_{\text{osc}}} \right)^2 \leq \left( \frac{\sigma_C}{C} \right)^2 + \max \left[ \frac{\sigma_{\text{CP,off}}}{V_{\text{IN}}} \right]^2 \left( \frac{V_{\text{LSB}} K'_{VCO}}{f_{\text{osc}}} \right)^2 \]  

in which, \( \sigma_f \), \( \sigma_C \), and \( \sigma_{\text{CP,off}} \), represent the standard deviation of the nominal operating frequency, C, and V CP,off, K’VCO is the VCO gain.

### III. CIRCUIT IMPLEMENTATION

According to (1), the frequency accuracy is determined by the capacitor tolerance, the comparator offset, the number of bits in D ctrl, and the VCO gain. As the capacitor tolerance is the dominant variation in the system, it is important to choose the optimal block implementation in the self-calibration system so that the contributions from other variation terms are minimized.

#### Time-to-Voltage Converter (TVC)

The TVC measures the oscillation period, and its absolute accuracy is especially critical. It is realized with a current source (I ref) charging up a pF capacitor, as illustrated in Fig. 3(a). CLK is generated by a divider after the VCO, and it has a 50-50 duty cycle and a period of 2NT osc. The output voltage V TVC at the end of each charging period equals LV ref T osc/C.
transistors were sized to be big, and the offset variation is small. To minimize input offset, the input is taken to force a bit-decision when the voltage difference at the active edge of the next comparison cycle sets it to zero.

The comparator can make decisions to high accuracy in less than 2ns. As a fail-safe option around meta-stability, provision is taken to force a bit-decision when the voltage difference at the input is extremely small. To minimize input offset, the input transistors were sized to be big, and the offset variation is simulated to be <1mV. An auto-zeroing preamp can further reduce it for higher accuracy applications.

Voltage-Controlled Oscillator (VCO)

The VCO is implemented with a three-stage current starved inverter chain ring oscillator. A wide tuning range is achieved through two identical bias current sources: one controlled by the MSB of D_in, and the other controlled by V ctrl generated by DAC using the rest of the bits in D_in. Corner simulation indicates an overlap of tuning ranges between 750 MHz and 2.2 GHz despite center frequency shifts due to variation.

Phase noise of the system is determined by the DAC and the VCO, as the rest of the circuitry is powered down and the feedback is cut off after the self-calibration is completed. It meets the relaxed phase noise specifications for the low power radio applications we proposed.

SAR and DAC

The SAR algorithm uses 11-Flops and 11-Muxs and starts with loading 0’s in all but the MSB flop where a 1 is loaded. In every successive update cycle, the 1 is shifted to the next flop while the bit comparison decisions from the comparator are stored, starting from MSB. It is auto-timed, and the conversion completion is indicated by the LSB flop (Q0) flips from 0 to 1.

IV. MEASUREMENT RESULTS

We fabricated the proposed oscillator in two different lots 6-month apart using TSMC’s 65nm CMOS process. A full set of 94 test chips are measured in both multi-project runs. The histograms of the measurements are presented in Fig. 5, which compare the normalized standard deviation (σ/µ) of the oscillator frequency without (free-running) and with self-calibration. At 3 different V_in, we are able to obtain the histograms exhibiting 3 different mean frequencies (0.85 GHz, 1.36 GHz, and 1.95 GHz). In all 3 cases, narrower die-to-die spread and smaller lot-to-lot shift in the mean frequency can be observed. The improvement factors defined by the ratio of σ/µ of the self-calibrated VCO over that of the free-running VCO are 4.9x (at 0.84 GHz), 4.41x (at 1.38 GHz) and 3.38x (at 1.96 GHz). Notice that accuracy decreases at higher frequency (i.e. lower V_in), as predicted by (1) in Section II.

To test the sensitivity of the self-calibrated VCO against the supply voltage, we sweep V_DD from 0.85V to 1.15V. Here, we set the operating frequency at 0.84 GHz, and define f_0 as the average frequency measured at nominal V_DD=1V for both the free-running and the self-calibrated VCO. Against this 30% supply variation, the free-running VCO on a typical chip varies...
by 72% around its center frequency, while the self-calibrated one experiences only 1.6% frequency deviation, yielding a 45x improvement as shown in Fig. 6. To gauge the combined effect of both process and VDD variation, we perform the same VDD sweep on the slowest and the fastest dies among all 94 test chips. Since process variation shifts the $\Delta f/f_0$ versus VDD curves upwards for the fast chip and downwards for the slow chip approximately by the amount of the worst frequency spread in the histograms, we have a worst case ±4% frequency deviation after self-calibration in Fig. 6(b), compared to -49% and +72% frequency deviation in the free-running ones in Fig. 6(a).

In Fig. 7, we measure the free-running and self-calibrated oscillators on a randomly-selected die over a temperature range from -7°C to 76°C and observe 5.2x improvement after self-calibration (1.32%) over the free-running one (6.88%).

The waveforms in Fig. 8 show the transitions between the Sleep/RST and the self-calibration at two different frequencies (0.84GHz and 1.38GHz). The duration of the self-calibration depends on the operating frequency. As indicated in Fig. 8, a single calibration requires between 250ns and 600ns and consumes between 60pJ and 135pJ. The difference of phase noise between the free-running and self-calibrated oscillators is negligible. At 1.38GHz with 10MHz offset frequency, both oscillators exhibit -98dBc/Hz spot phase noise. A summary of the self-calibrated VCO design specs and PVT accuracy is included in Table I. The die photo and zoomed-in layout are shown in Fig. 9. The core area of the VCO and the self-calibration circuitry occupy 0.06mm².

Table II compares our work with other oscillator designs in the literature. The tunable GHz operating frequency and the frequency accuracy of our design allows dual functions as both local oscillator [3] and system clock [1] in low power radios. Compared to [3] at GHz range, our design shows much improved PVT-invariance with small power overhead. The oscillator presented in [1] operates at kHz range while consuming similar amount of power. It requires frequency trimming and additional high-precision temperature sensors to achieve the temperature sensitivity of 103ppm°C, which is

![Fig. 5. Comparison of output frequency histograms without (free-running) and with the proposed self-calibration at different frequencies: (a) and (b) 0.84GHz; (c) and (d) 1.38GHz; (e) and (f) 1.96GHz.](image)

![Fig. 6. Measured percentage deviation from the nominal frequency at different supply voltages (VDD) in (a) the free-running and (b) the self-calibrated oscillators.](image)

![Fig. 7. Measured frequency deviation at different temperature before and after the calibration.](image)
Dependent on the operating frequency.

**Fig. 8.** Output oscillation waveforms (divided down by 32) of two consecutive self-calibrations at (a) 0.84GHz and (b) 1.38GHz.

TABLE I: CHIP SUMMARY

|---------|----------------|-----------|-------------|--------------|----------|------|--------
| TSMC 65nm CMOS | 1V | 0.8~2GHz | 250~680ns | 60~135pJ | 2.24% | 0.06mm² | 46µW

**TABLE II**

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<tr>
<td>65nm CMOS</td>
<td>1V</td>
<td>0.8~2GHz</td>
<td>Single-point current calib.</td>
<td>&lt;10%</td>
<td>-5°C~75°C</td>
<td>ppm/°C</td>
<td>0.85V~1.15V</td>
<td>1.6%</td>
<td>46µW</td>
<td>0.06mm²</td>
<td>94</td>
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<td>2GHz</td>
<td>Single-point freq. calib.</td>
<td>0%</td>
<td>0°C~90°C</td>
<td>ppm/°C</td>
<td>0.9V~1.1V</td>
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<td>1GHz</td>
<td>Multi-point calib.</td>
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<td>22°C~85°C</td>
<td>ppm/°C</td>
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<td>0.27mm²</td>
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* Not measurement data. **Compared to the PVT calibrator in [15].*** Only 1 chip is measured.

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**REFERENCES**


